Claims

1. A logic simulation hardware emulator, comprising:

a simulation model comprising one or more source emulation processors coupled to one or more receiving emulation processors by an emulation cable having a plurality of signal wires, the plurality of signal wires comprising a plurality of regular signal wires and one or more spare signal wires; and

a runtime control program for controlling the simulation model, wherein upon detection of a fault on a regular signal wire, the runtime control program reassigns a signal on the regular signal wire having the fault to the one or more spare signal wires.

2. The logic simulation hardware emulator of claim 1, wherein the one or more spare signal wires are defined at simulation model build time.

3. The logic simulation hardware emulator of claim 3, wherein the one or more spare signal wires are defined by designating one or more emulation processors and their corresponding regular signal wires as faulty during simulation model build.

4. The logic simulation hardware emulator of claim 1, wherein the logic simulation hardware emulator further comprises a spare select multiplexer, the inputs of the spare select multiplexer coupled to the outputs of the one or more source emulation processors, and output of the spare select multiplexer coupled to the input of the emulation cable, wherein the spare select multiplexer multiplexes the signal on the regular signal wire having the fault through the one or more spare signal wires.

5. The logic simulation hardware emulator of claim 4, wherein a signal select for the spare select multiplexer is provided by a spare select register.

6. The logic simulation hardware emulator of claim 5, wherein the spare select register is updated by the runtime control program during the simulation run.

7. The logic simulation hardware emulator of claim 1, wherein the simulation hardware emulator further comprises:

one or more source type multiplexers coupled to an output of the emulation cable, wherein each of the source type multiplexers has a select signal; and

a plurality of processor selector multiplexers coupled to the outputs of the one or more source type multiplexers, wherein the output of each processor selector multiplexer is coupled to an input of one or more receiving emulation processors, and wherein each of the processor selector multiplexers has a select signal.

8. The logic simulation hardware emulator of claim 7, wherein the select signals for the source type multiplexer and the processor selector multiplexer are provided by the runtime control program.

9. A method for the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors coupled to one or more receiving emulation processors by a set of emulation cables, each emulation cable having a plurality of signal wires; the plurality of signal wires comprising a plurality of regular signal wires and one or more predefined spare signal wires, the method comprising the steps of:

identifying a set of faulty signal wires within the plurality of regular signal wires, if any faulty signal wires exist; and

reassigning signals from the set of faulty signal wires to the one or more spare signal wires within the set of emulation cables.

10. The method of claim 9, wherein the method further includes the step of:

performing a connectivity diagnostic on the set of emulation cables within the hardware emulator.

11. The method of claim 9, wherein the method further includes the step of:

predefining one or more spare signal wires within the emulation cables at simulation model build time.

12. The method of claim 9, wherein the step of reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables includes the steps of:

determining if a spare signal wire is available, if one or more faulty signal wires exist;

setting a source module spare register to a value corresponding to the source emulation processor having the faulty wire; and

changing any receiving emulation processor steps sourced by the faulty wire to the spare wire.

13. A computer-readable program stored on a computer-readable medium, the computer readable program providing the automatic reconfiguration of faulty signal wires in a logic simulation hardware emulator, the logic simulation hardware emulator having one or more source emulation processors coupled to a one or more receiving emulation processors by a set of emulation cables, each emulation cable having a plurality of signal wires; the plurality of signal wires comprising a plurality of regular signal wires and one or more predefined spare signal wires, the computer readable program being configured to perform the steps of:

identifying a set of faulty signal wires within the plurality of regular signal wires, if any faulty signals wires exist; and

reassigning signals from the set of faulty signal wires to the one or more spare signal wires within the set of emulation cables.

14. The computer-readable program of claim 13, wherein the computer-readable program further includes the step of:

performing a connectivity diagnostic on the set of emulation cables within the hardware emulator.

15. The computer-readable program of claim 13, wherein the method further includes the step of:

predefining one or more spare signal wires within the emulation cables at simulation model build time.

16. The computer-readable program of claim 13, wherein the step of reassigning signals from the set of faulty signal wires to one or more spare signal wires within the set of emulation cables includes the steps of:

determining if a spare signal wire is available, if one or more faulty signal wires exist;

setting a source module spare register to a value corresponding to the source emulation processor having the faulty wire; and

changing any receiving emulation processor steps sourced by the faulty wire to the spare wire.